

Highlights

- (6) Tri-Speed Ports w/ Layer 2/3 Switch Management
- IRIG-A/B/G Time Code Generator
- (1) IRIG DC Input, (2) IRIG DC/1PPS Outputs & (2) IRIG AM Outputs
- (1-4) Hardware IEEE-1588v2 Clocks
- Programmable Discrete Inputs/Outputs



Overview

The iES-6 integrated Ethernet Switch, is a rugged 6 port layer 2/3 managed gigabit Ethernet switch with end node timing & discrete signal capabilities for demanding test instrumentation environments on airborne, shipboard or mobile ground vehicles.

Programmable discrete outputs can be used to control end node devices, on or off the network, as well as feedback into the iES-6 from discrete inputs.

iES-6 contains a hardware based IEEE-1588v2 time engine with (4) independent clocks which can be setup as ordinary, boundary, peer to peer transparent or end to end transparent, master only, slave only & one or two step clock. A Grand Master clock capability is available on the iES-12 & iES-16. The hardware timer in the MAC, provides (20) nanosecond accuracy & (4) nanosecond resolution.

The iES-6 contains a Content-Aware Packet Processor for wire speed packet inspection of advanced VLAN & QoS classifications/manipulations, IP source guarding, & security features. These are just a few of the types of inspections which can be performed. Selected ingress traffic can be applied across the iES-6 or per port. There are several methods of configuring traffic filtering, port use limit control, VLAN/MAC address, packet/rate limiters, port based & frame type.

PTP Clock's Configuration

Local Clock Current Time	Clock Adjustment method	Synchronize to System Clock	Ports Configuration
1970-01-01T00:00:38+00:00 267,425,440	Internal Timer	Synchronize to System Clock	Ports Configuration

Clock Default Data Set

ClockId	Device Type	2 Step Flag	Ports	Clock Identity	Dom	Clock Quality	Pri1	Pri2	Protoco
0	Ord-Bound	True	8	30:2d:e8:ff:fe:11:12:34	0	Cl:251 Ac:Unknwn Va:65535	128	128	Ethernet

Clock Current Data Set

stpRm	Offset From Master	Mean Path Delay	Filter Parameters
0	0.000,000,000	0.000,000,000	DelayFilter: 6, period: 1, dist: 2

Clock Parent Data Set

Parent Port Identity	Port	PStat	Var	ChangeRate	Grand Master Identity	Grand Master Clock Quality	Pri1	Pri2
30:2d:e8:ff:fe:11:12:34	0	False	0	0	30:2d:e8:ff:fe:11:12:34	Cl:251 Ac:Unknwn Va:65535	128	

Clock Time Properties Data Set

UtcOffset	Valid	leap59	leap61	Time Trac	Freq Trac	ptp Time Scale	Time Source
0	False	False	False	False	False	True	160

Servo Parameters

Display	P-enable	I-enable	D-enable	'P' constant	'I' constant	'D' constant
False	True	True	True	3	90	

Unicast Slave Configuration

Index	Duration	ip address	grant	CommSta
0	100	0.0.0.0	0	IDLE
1	100	0.0.0.0	0	IDLE
2	100	0.0.0.0	0	IDLE
3	100	0.0.0.0	0	IDLE
4	100	0.0.0.0	0	IDLE

Specifications @ telspandata.com/iES6

- Non-Blocking Wire Speed Performance for All Frame Sizes Up to 9.6KB
- 4K VLAN's, 256 Filtering Policies
- 8K L2 Multicast Groups Addresses
- Port Mirroring, Link Aggregation
- CLI, Web GUI or SNMP Command, Control & Monitoring
- RS-232 COM Port



Highlight Specifications



28VDC
MIL-STD-704A



Width 5.17"
Length 7.15"
Height 2"



MIL-STD-810F
Shock/Vibe/
Gun Fire/Sand
Rain/+ More



3 Pounds



-40C to +75C
MIL-STD-810F



(6) 10/100/1000
Ethernet Ports
Layer 2/3
Managed



IRIG A/B/G
1PPS, DC & AM
IEEE-1588v2
Master, Slave



RS-232



6 Outputs
1 Reset

Full Specifications @ telspandata.com/iES6