

## Highlights

- 12 Tri-Speed Ports w/ Layer 2/3 Management
- Programmable FPGA w/ two 1Gbps Switch Interfaces
- HDLC/Chapter 7 PCM Encoder/Decoder
- GPS Receiver & IRIG-A/B/G Time Code Generator
- 3 IRIG DC/1PPS Outputs & 3 IRIG AM Outputs
- Up to (4) IEEE-1588v2 Clocks w/ Grand Master Capability
- Up to 16 Programmable Discrete Inputs/Outputs

## Overview

The integrated Ethernet Switch (iES-12), is a rugged 12 port layer 2/3 managed gigabit Ethernet switch with end node timing, discrete signal capabilities for demanding environments on airborne, shipboard & ground vehicles.



A programmable FPGA tied directly into the switch with two 1G interfaces provides packet processing capabilities. Programmable or data driven discrete outputs can be used to control end node devices, on or off the network, as well as feedback into the iES-12 from discrete inputs. The FPGA also provides built-in HDLC & IRIG 106 Chapter 7 PCM encoder & decoder. This allows PCM output of VLAN, mirrored or filtered Ethernet switch traffic or from the PCM input decoded Ethernet back out the switch Ethernet ports.

With multiple time sources and outputs the iES-12 provides end node device IRIG time signals. iES-12 contains a high time accuracy internal GPS receiver & a hardware based IEEE-1588v2 time engine both able to drive the internal IRIG-A/B/G Time Code Generator (TCG) for time outputs.

**Telspan Data** integrated Ethernet Switch, iES-12™

Configuration

- System
  - Green Ethernet
  - Thermal Protection
  - Ports
  - Security
  - Aggregation
  - Link OAM
  - Loop Protection
  - Spanning Tree
  - IPMC Profile
    - MVR
    - IPMC
    - LLDP
    - SyncE
    - EPS
    - MEP
    - ERPS
    - MAC Table
    - VLAN Translation
    - VLANs
    - Private VLANs
    - VCL
    - Voice VLAN
  - Ethernet Services
    - QoS
    - Mirroring
    - UPnP
    - PTP
    - sFlow
    - FPGA
      - .1588
      - RESET
      - DISCRETE
      - TIMIN
      - TIMOUT
      - EPE
  - Monitor
  - Diagnostics
    - Ping
    - Link OAM
    - MIB Retrieval
    - Port

**PTP Clock's Configuration**

Local Clock Current Time

PTP Time	Clock Adjustment method	Synchronize to System Clock	Ports Configuration
1970-01-01T00:04:58+00:00 331.724.720	Internal Timer	Synchronize to System Clock	Ports Configuration

Clock Default DataSet

ClockId	Device Type	2 Step Flag	Ports	Clock Identity	Dom	Clock Quality	Pri1	Pri2	Protocol
0	Ord-Bound	True	14	30:2d:e8:ff:fe:11:12:34	0	Cl:251 Ac:Unkwn Va:65535	128	128	Ethernet

Clock Current DataSet

stpRm	Offset From Master	Mean Path Delay
0	0.000,000,000	0.000,000,000

Filter Parameters

DelayFilter	period	dist
6	1	2

Clock Parent DataSet

Parent Port Identity	Port	PStat	Var	ChangeRate	Grand Master Identity	Grand Master Clock Quality	Pri1	Pri2
30:2d:e8:ff:fe:11:12:34	0	False	0	0	30:2d:e8:ff:fe:11:12:34	Cl:251 Ac:Unkwn Va:65535	128	128

Clock Time Properties DataSet

UtcOffset	Valid	leap59	leap61	Time Trac
0	False	False	False	False

Servo Parameters

Display	P-enable	I-enable	D-enable	'P'
False	True	True	True	3

Unicast Slave Configuration

Index	Duration	ip_address	grant	C
0	10	192.168.1.1	0	
1	100	0.0.0.0	0	
2	100	0.0.0.0	0	
3	100	0.0.0.0	0	IDLE
4	100	0.0.0.0	0	IDLE

Save Reset

## Specifications @

[telspandata.com/iES12](https://telspandata.com/iES12)

- Non-Blocking Wire Speed Performance for All Frame Sizes Up to 9.6KB
- FPGA for data processing, filtering & HDLC/CH7 PCM input/output
  - 4K VLAN's, 256 Filtering Policies
  - 8K L2 Multicast Groups Addresses
  - Port Mirroring & Link Aggregation
  - CLI, Web GUI or SNMP Control & Monitoring
  - RS-232 COM Port